CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A memory array comprises:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor and a first underlying capacitor that are in electrical contact to each other through a first buried strap, said first buried strap positioned on a first collar region; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor and a second underlying capacitor that are in electrical contact to each other through an offset buried strap, said offset buried strap positioned on a second collar region, wherein said second collar region has a length equal to said first collar region.

2. The memory array of Claim 1 further comprising:

at least one other-type memory device, each of said at least one other-type memory device comprises another transistor and another underlying capacitor that are in electrical contact to each other through a further-offset buried strap, said further-offset buried strap positioned on another collar region, wherein said another collar region has a length equal to said second collar region and said first collar region.

3. The memory array of Claim 1, wherein said first buried strap region and said offset buried strap region are offset by a vertical dimension ranging from about 0.4 μm to about 0.6 μm.

4. The memory array of Claim 1, wherein said first underlying capacitor comprises at least one first-bottling region and said second underlying capacitor comprises at least one offset-bottling region.

5. The memory array of Claim 1, further comprising a support region.

6. The memory array of Claim 1, wherein said at least one first-type memory device is formed within a first trench; and said at least one second-type memory cell is formed within a second trench.

7. The memory array of Claim 6, wherein, said first trench has a depth ranging from about 1 μm to about 10 μm and said second trench has a depth ranging from about 1 μm to about 10 μm.

8. The memory array of Claim 1 wherein a first bottom surface of said first collar region is vertically offset from a second bottom surface of said second collar region.

9. The memory array of Claim 8 wherein said first bottom surface is vertically offset from said second bottom surface by a dimension ranging from about 0.4 μm to about 0.6 μm.

10. The memory array of Claim 1 wherein said first underlying capacitor and said second underlying capacitor have a vertical orientation.

11. A method of forming a memory array comprising:

etching a substrate to provide a first trench having an initial depth and a second trench having an intermediate depth to produce an offset in a vertical dimension between said first trench region and said second trench region;

forming sacrificial sidewall spacers to said initial depth of said first trench and to said intermediate depth of said second trench;

etching said first trench to a first collar depth and said second trench to a second collar depth, wherein said offset between said first trench and said second trench is maintained;

forming collars within said first trench and said second trench, said collars positioned underlying said sacrificial sidewall spacers within said first trench and said second trench;

forming capacitors in said first trench and said second trench, each of said capacitors extending above a bottom surface of said collars;

recessing said collars below a top surface of said capacitors, wherein recessed collars in said first trench and said second trench are of equal length;

forming buried straps atop said recessed collars in said first trench and said second trench, wherein said buried straps of said first trench are separated from said buried straps of said second trench by said offset in said vertical dimension; and

forming transistors atop said capacitors in said first trench and said second trench.

12. The method of Claim 11 wherein said etching said substrate to provide said first trench having said initial depth and said second trench having said intermediate depth further comprises:

providing a film stack atop said substrate;

patterning said film stack to expose regions of said substrate where said first trench and said second trench are subsequently formed;

applying a block mask atop said regions of said substrate where said first trench is subsequently formed and etching said second trench;

stripping said block mask; and

etching said second trench to said intermediate depth and said first trench to said initial depth.

13. The method of Claim 11 wherein said collars are formed by local oxidation of silicon.

14. The method of Claim 11 wherein forming said capacitors further comprises:

etching said first trench to a first capacitor depth and said second trench to a second capacitor depth, wherein said offset between said first trench and second trench is maintained;

depositing a node dielectric within said first trench and said second trench;

forming polysilicon within said first trench and said second trench;

recessing said polysilicon until said polysilicon within said first trench is recessed below a top surface of said collar within said first trench;

applying a block mask atop said first trench region; and

recessing said polysilicon within said second trench until said polysilicon is recessed below a top surface of said collar within said second trench.

15. The method of Claim 11 wherein said capacitors further include bottled regions formed by an etch process having selective alternating anisotropic and isotropic etch properties.

16. The method of Claim 11 wherein said recessing said collars comprises:

removing said sacrificial sidewall spacers and an upper portion of said node dielectric by selective etch; and

selectively etching said collars to produce divots in said first trench and said second trench, wherein said divots within said first trench are separated from said divots within said second trench by said offset in said vertical dimension.

17. The method of Claim 16 wherein said forming said buried straps comprises:

depositing strap polysilicon within said first trench and said second trench; and

etching back said strap polysilicon, wherein a remaining portion of said strap polysilicon is positioned within said divots.

18. The method of Claim 11 further comprising a trench top oxide positioned between said capacitors in said first trench and said second trench and said transistors in said first trench and said second trench.

19. The method of Claim 11 wherein said forming said transistors comprises:

forming gate dielectrics on exposed sidewalls of said first trench and said second trench;

forming gate regions within said first trench and said second trench;

doping said substrate atop said buried straps to provide a channel; and

doping said substrate atop said channel to provide a drain.

20. The method of Claim 11 further comprising forming another trench having another offset buried strap atop equal length collars electrically connecting another transistor to another capacitor.